IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

VLSI TECHNOLOGY LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	Case No. 6:21-cv-00057-ADA [redacted]

DEFENDANT INTEL CORPORATION'S RESPONSE TO VLSI TECHNOLOGY LLC'S MOTION FOR LEAVE TO FILE SURREPLIES IN OPPOSITION TO INTEL'S RULE 50(B) AND RULE 59 MOTIONS

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Page(s)

CASES

STATUTES AND RULES

I. INTRODUCTION

Throughout this litigation, VLSI has strategically withheld substantive positions on issues and disrupted the orderly process of this case. Indeed, as detailed in Intel's unclean hands brief, VLSI adopted this approach in its infringement contentions, expert reports, and trial presentation. (*See* Dkt. 590 at 15-18.) VLSI's motion for leave to file surreplies in opposition to Intel's post-trial briefs is the latest example of these litigation tactics. After stipulating to a post-trial briefing schedule that did not contemplate surreply briefs, VLSI has now moved for leave to submit surreplies that include numerous arguments that VLSI repeats from its earlier responses or that VLSI could have raised in its responses but chose not to do so. This Court should not reward VLSI's maneuvers and permit it to effectively redo its responsive briefing, particularly because its justifications for seeking leave to file surreplies are conclusory and cite no support. There is no basis for VLSI's surreplies, and this Court should deny VLSI's motion.

II. VLSI HAS NOT COME CLOSE TO MEETING THE HIGH BURDEN TO JUSTIFY ITS SURREPLIES.

The law in this district is clear that "surreplies are 'highly disfavored' and permitted only in 'extraordinary circumstances.'" *Manchester Texas Fin. Grp. v. Badame*, No. A-19-CV-00009-LY, 2019 WL 4228370, at *1 n.1 (W.D. Tex. Sept. 4, 2019). VLSI's barebones motion, which does not cite a single case or fact in support, does not come close to meeting that high bar. *See Silo Rest. Inc. v. Allied Prop. & Cas. Ins. Co.*, 420 F. Supp. 3d 562, 571 (W.D. Tex. 2019) (denying motion for leave where plaintiff failed to "show[] exceptional or extraordinary circumstances that warrant a surreply"). Indeed, VLSI offers just a single sentence of conclusory, unsupported assertions as purported justification for its surreplies. (Dkt. 629 ¶ 2.) Each assertion is meritless and fails to establish that "extraordinary circumstances" justify granting VLSI's request for leave.

First, VLSI asserts that the "nature and complexity of the issues" justify surreply briefing. (Dkt. 629 ¶ 2.) As an initial matter, VLSI does not identify any authority authorizing a surreply due to alleged "complexity," and Intel is aware of none. Moreover, VLSI never identifies the purported "complexities" that require additional briefing nor explains why the issues presented in Intel's motion—noninfringement, invalidity, and damages—are more complex than in any other patent case or necessitate a surreply. In any event, VLSI knew of any purported "complexities" when the parties stipulated to a post-trial briefing schedule in April 2021. (*See* Dkt. 587.) Yet VLSI did not seek to include surreplies to Intel's Rule 50(b) and 59 motions in that agreed schedule, despite being well aware of the issues.

Second, VLSI argues that there exist "numerous inaccuracies" and "new arguments" in Intel's replies that justify its surreplies. (Dkt. 629 ¶ 2.) Again, VLSI does not identify in its motion any purported "inaccuracies" or "new arguments" to support its claim. *See Silo Rest. Inc.*, 420 F. Supp. 3d at 571 ("[I]n seeking leave to file a surreply brief, a party ***must identify*** the new issues, theories, or arguments which the movant raised for the first time in its reply brief." (emphasis added)). And as explained below, Intel's replies do not contain any inaccuracies or new arguments. Instead, Intel properly responded to arguments raised in VLSI's responses, including by citing evidence in the record to support its reply. In any event, purported "inaccuracies" are not proper grounds for a surreply. *See Racetrac Petrol., Inc. v. J.J.'s Fast Stop, Inc.*, No. CIV.A. 3:01-CV-1397, 2003 WL 251318, at *21 (N.D. Tex. Feb. 3, 2003) (rejecting motion for leave to file surreply to address purported "factual inaccuracies," noting that "Plaintiff simply wants an opportunity to continue the argument[, which] is not permitted").

As this district has recognized, one party has to be given the last word. *See Davis v. United Health Servs.*, No. 1:18-CV-1093-RP, 2020 WL 33597, at *3 (W.D. Tex. Jan. 2, 2020)

("The purpose for having a motion, response, and reply is to give the movant the final opportunity to be heard." (quoting *Racetrac*, 2003 WL 251318, at *18)). Here, Intel, as the movant, is entitled to the last briefs on its JMOL and new trial motions. *Id.* VLSI's motion for leave demonstrates no extraordinary circumstances to justify subverting this standard process. Accordingly, leave to file surreplies should be denied on this basis alone.

III. VLSI'S PROPOSED SURREPLIES CONFIRM THAT LEAVE TO FILE SHOULD NOT BE GRANTED.

A. VLSI's Rule 50(b) Surreply Does Not Identify Any New Or Allegedly Inaccurate Arguments That Justify A Surreply.

VLSI's Rule 50(b) surreply recycles arguments from its Rule 50(b) response and includes arguments that VLSI could have made—but failed to make—in its earlier brief. VLSI's surreply thus confirms that this Court should deny VLSI's motion for leave.

1. VLSI's Rule 50(b) surreply confirms there is no basis for a surreply regarding noninfringement of the '373 patent.

For the '373 patent, although VLSI insists that Intel's reply demands a substantive response, VLSI fails to substantively address any aspect of Intel's arguments. Instead, VLSI recycles evidence and arguments from its responsive brief, while ignoring most of Intel's reply—a selective approach illustrating that VLSI's goal is not to sharpen the arguments for the Court but instead to have the last word. With one exception,[1] all the exhibits and testimony cited in the portion of VLSI's surreply concerning the '373 patent were previously cited in VLSI's response (and then addressed in Intel's reply).

[1] The only new testimony that VLSI cites is Mr. Borkowski's discussion of demonstrative DDX-5.6, contrasting that testimony with Dr. Conte's discussion of D-505. (Dkt. 629-1 at 3 (citing Sealed Tr. [Borkowski] 105:8-107:23).) It is unclear what purpose this argument serves, as it ignores the observation in Intel's reply that VLSI's reliance on D-505 is ***generally*** improper, because VLSI introduced no evidence and asked no questions of Intel's engineers about whether D-505 reflected the final design of the accused products—providing no basis for the jury to rely on it as corroboration for Dr. Conte's conclusory testimony. (Dkt. 615 at 3 n.3.)

With respect to the "minimum operating voltage" limitations, VLSI merely repeats the arguments raised in its opposition concerning the evidence purportedly supporting Dr. Conte's opinion that RING_RETENTION_VOLTAGE is the minimum operating voltage of the C6 SRAM. (*Compare* Dkt. 603 at 1-6 (Opposition), *with* Dkt. 629-1 at 1-4 (Surreply).) In rehashing these arguments, VLSI sidesteps Intel's arguments that VLSI impermissibly relies on its expert's *ipse dixit*, violating the principle that conclusory testimony cannot sustain a jury's verdict. (Dkt. 615 at 2 (citing *Guile v. United States*, 422 F.3d 221, 227 (5th Cir. 2005); *Wisconsin Alumni Research Found. v. Apple Inc.*, 905 F.3d 1341, 1349-50 (Fed. Cir. 2018)).[2] In short, VLSI's proposed surreply merely ties together the ***same exhibits*** using the ***same conclusory testimony***. By ignoring Intel's key arguments, VLSI's proposed surreply would add nothing to the Court's consideration of Intel's motion.

Similarly, VLSI offers no justification for a surreply concerning the "when" limitations of the '373 patent. VLSI claims that Intel has "abandon[ed]" its noninfringement theory that "'the RING_RETENTION_VOLTAGE fuse value is [not] ever used to guide "when"' voltages are supplied" to the C6 SRAM. (Dkt. 629-1 at 4-6.) VLSI is incorrect. Intel expressly ***defended*** that theory in its reply, noting that "Intel's argument simply reflects the plain meaning of the 'when' limitations, which set forth ***two conditions*** connected to the relationship between the stored minimum operating voltage and the first regulated voltage." (Dkt. 615 at 4 (emphasis added).) VLSI also insists that Intel has now raised a "new argument" concerning the conditions under which VCCR is supplied to the C6 SRAM. (Dkt. 629-1 at 5.) This too is wrong. The

[2] VLSI ignores Intel's other arguments regarding the record evidence concerning the "minimum operating voltage" limitations, including Dr. Conte's admission that he never analyzed whether the components in the ring domain (including the C6 SRAM) actually operate (or are capable of operating) at voltage values below RING_RETENTION_VOLTAGE (Dkt. 615 at 1), as well as the fact that RING_RETENTION_VOLTAGE is not specific to the C6 SRAM (*id.* at 1-2 & n.2).

supposedly "new" argument came in response to VLSI's false claim that "Dr. Conte confirmed Intel's chips do, in fact, use the RING_RETENTION_VOLTAGE in selecting which voltage source to use for the C6 SRAM." (Dkt. 603 at 8.) In its reply, Intel explained that the record did not support this claim[3] and cited Dr. Conte's ***own*** contrary testimony. (Dkt. 615 at 3 (citing Sealed Tr. [Conte] 83:17-84:20).) And—as relevant to VLSI's claim—Intel observed that even if Dr. Conte ***had*** made such a claim, it would have been contrary to the uncontroverted evidence that the voltage conditions for the C6 SRAM can be "the ***opposite*** of what the claims require." (*Id.* at 4.)

Finally, VLSI does not even allege that its surreply argument regarding the "while" limitations is in response to a purportedly new argument. Instead, VLSI simply offers a single conclusory sentence that relies entirely on its response brief (Dkt. 629-1 at 6), thus confirming the impropriety of VLSI's surreply.

2. VLSI's Rule 50(b) surreply confirms there is no basis for a surreply regarding noninfringement or invalidity of the '759 patent.

For the '759 patent, VLSI seeks to rewrite its equivalents theory and contend that its expert Dr. Conte did not assert any equivalent for the claimed "request." (Dkt. 629-1 at 6.) But as explained in Intel's opening brief, Dr. Conte agreed that "C0 residency data is the required request from the claims … [i]n the DOE argument." (Dkt. 591 at 9-10; *see* Dkt. 615 at 5-7.) Indeed, Intel cited this exact testimony in its opening brief (Dkt. 591 at 9-10), and VLSI does not even attempt to suggest this is a "new argument" that warrants a surreply. Thus, the entirety of

[3] VLSI claims that "Dr. Conte's cited testimony speaks for itself." (Dkt. 629-1 at 5-6 (citing Sealed Tr. [Conte] 15:10-16:6).) That testimony does "speak[] for itself"—but not in VLSI's favor. On the contrary, just as Intel explained in its reply, the testimony provides no support for Dr. Conte's claim. (Dkt. 615 at 3-4.) Dr. Conte said nothing about the RING_RETENTION_VOLTAGE fuse value being "***used***" to set the state of the power multiplexer—his testimony lacked any causal connection between the fuse value and the multiplexer. (*Id.*)

VLSI's surreply argument could have—and should have—been raised in its response.[4] In any case, VLSI's discussion of C0 residency counters (Dkt. 629-1 at 6-7) is a sideshow and contradicted by Dr. Conte's confirmation, quoted above, that he relied on C0 residency ***data***—not C0 residency counters—as the claimed "request" in his equivalents theory. VLSI's attempt to confuse the issues by suggesting that Dr. Conte's reference to C0 residency data was actually a reference to Core_Active signals and C0 residency counters again conflates his literal infringement theory with his doctrine of equivalents theory. (Dkt. 615 at 5-6.) The Court should disregard VLSI's post-hoc attempt to rewrite Dr. Conte's opinions in surreply.

VLSI dedicates a single sentence to the argument regarding the "output to control" limitation that does nothing more than cite VLSI's response brief. (Dkt. 629-1 at 7.) Likewise, VLSI includes a single-sentence response to Intel's argument regarding invalidity of the '759 patent, but this sentence also does nothing more than cite VLSI's response brief. (Dkt. 629-1 at 7.) These arguments are meritless (Dkt. 615 at 7-9) and, in any event, are not a proper basis for a surreply.

3. VLSI's Rule 50(b) surreply confirms there is no basis for a surreply regarding damages.

VLSI's arguments regarding damages also rely almost exclusively on its original responses to Intel's motion. (Dkt. 629-1 at 7-8.) For example, VLSI's surreply simply extends its response briefing by continuing to assert that "Dr. Sullivan's damages numbers absolutely are in the record" (*id.* at 8), even though the record shows Dr. Sullivan's damages numbers were never put into evidence (Dkt. 591 at 18-19; Dkt. 615 at 10). Wanting to have the last word or to further develop an argument, however, is not an "extraordinary circumstance" that justifies leave

[4] VLSI made nearly identical arguments in its response to Intel's Rule 52 motion regarding the '759 patent, confirming that VLSI could have offered the same response to Intel's Rule 50(b) motion but simply chose not to. (*See* Dkt. 607 at 3-6 & n.1, 19-20.)

to file a surreply brief. *Silo Rest. Inc.*, 420 F. Supp. 3d at 570-71 (noting that "surreplies often amount to little more than a strategic effort by the nonmovant to have the last word on a matter," which does not constitute "exceptional or extraordinary circumstances warranting" a surreply). Worse still, VLSI's surreply brief includes belated damages arguments that VLSI could have raised in its response brief but chose not to, including its new assertion that "Dr. Sullivan showed the jury the exact calculations and resulting royalties." (Dkt. 629-1 at 8.) This argument is not only procedurally improper, but it also does not respond to the position Intel actually advanced in its motion and reply. Indeed, even in its surreply, VLSI does not dispute Intel's showing that Dr. Sullivan's damages ***totals*** were never put into evidence. Instead, VLSI now alleges that "the exact calculations" required to derive those totals were before the jury—even though VLSI points only to demonstratives, which are not evidence and cannot support its argument. *See Whitserve, LLC v. Comput. Packages, Inc.*, 694 F.3d 10, 33 n.16 (Fed. Cir. 2012) ("When parties rely on demonstratives to present evidence or mathematical calculations to the jury, it is their burden to assure that the record captures the substance of the data so presented. We can not guess at what the jury saw.").[5]

B. VLSI's Rule 59 Surreply Does Not Identify Any New Arguments That Justify A Surreply.

Like its Rule 50(b) surreply, VLSI's Rule 59 surreply also recycles arguments from its Rule 59 response and includes arguments that VLSI could have made—but failed to make—in

[5] VLSI asserts that "Intel's own confidentiality objection to those numbers being read aloud has absolutely no bearing on their extensive evidentiary support." (Dkt. 629-1 at 8.) But the "numbers" VLSI is referring to are Intel's total accused revenues, which were, in fact, entered into evidence (over Intel's objection). (2/24 Tr. [Sullivan] 652:9-658:2; PDX7.49; PDX7.53; PTX-3903; PTX-3904.) Contrary to VLSI's suggestion, it was ***VLSI—***and ***not Intel***—that asserted that Dr. Sullivan's final damages totals were confidential.

its earlier response.[6] VLSI's Rule 59 surreply thus confirms that this Court should deny VLSI's motion for leave.

1. VLSI's Rule 59 surreply confirms there is no basis for a surreply regarding the noncomparable Intel agreements.

With respect to the admission of noncomparable agreements, VLSI's surreply consists of rehashed arguments from its response brief and new arguments that VLSI could have included—but chose not to include—in its response. (Dkt. 629-2 at 1-2.) VLSI's repeated arguments continue to sidestep the well-established law that noncomparable licenses cannot rebut evidence regarding comparable licenses. (Dkt. 594 at 1-6; Dkt. 614 at 1-3.) Moreover, these arguments are just an extension of the response brief and not proper surreply.

Beyond its rehashed arguments, VLSI introduces an entirely new argument regarding the purchase prices of sports franchises. (Dkt. 629-2 at 1-2.) But VLSI's assertion does not provide a justification for VLSI's introduction of irrelevant and highly prejudicial noncomparable licenses. (Dkt. 594 at 1-6; Dkt. 614 at 1-3.) Indeed, Intel's questioning of Dr. Sullivan had nothing to do with the comparable licenses relied on by Intel, and instead showed that Dr. Sullivan's damages numbers were "astronomical" by his own account. (2/24 Tr. [Sullivan] 701:2-7.)

2. VLSI's Rule 59 surreply confirms there is no basis for a surreply regarding Dr. Sullivan's damages theory.

With respect to Dr. Sullivan's damages theory, instead of responding to any allegedly new arguments (of which there are none), VLSI again uses its surreply to repeat arguments raised in its response while also responding for the first time to arguments raised in Intel's

[6] VLSI asserts in a footnote that "Intel misrepresents throughout its reply brief that VLSI 'concedes' or 'does not dispute' numerous assertions that VLSI plainly disputes." (Dkt. 629-2 at 1 n.1.) Tellingly, however, VLSI's footnote is devoid of any citations or identification of any such misrepresentations. Indeed, much of VLSI's surreply appears to be dedicated to disputing issues that VLSI failed to dispute in its original response.

opening brief. (Dkt. 629-2 at 2-6.) None of this justifies a surreply. For example, VLSI attempts to distinguish *Stragent, LLC v. Intel Corp.*, 2014 WL 1389304 (E.D. Tex. Mar. 6, 2014), even though Intel relied on *Stragent* in its opening brief (Dkt. 594 at 7-8) and VLSI already provided the same counterargument in its response (Dkt. 606 at 7). Likewise, regarding the entire market value rule, VLSI repeats arguments from its prior briefing without explaining why it could not have made these arguments earlier. (Dkt. 629-2 at 5-6.)[7]

Where VLSI purports to identify a new argument regarding its improper 100-to-0 profit split, VLSI is in fact mischaracterizing Intel's position. Contrary to VLSI assertion, Intel never argued that it is "not 'legally permissible' to ***consider*** Intel's infringing profits" at all. (*Id.* at 4.) In reality, Intel argued that it was improper for VLSI to ***base its damages entirely on Intel's profits*** and apply an improper profit-sharing theory that essentially amounted to disgorgement. (Dkt. 614 at 5-6.) There was nothing new about Intel's argument, as Intel raised Dr. Sullivan's improper profit-sharing theory in its opening brief (Dkt. 594 at 8.), and VLSI does not explain why an additional response is necessary. Indeed, VLSI's surreply does not actually respond to Intel's argument; nor could it, as VLSI cannot deny that its attempted disgorgement of Intel's profits is legally impermissible.

3. VLSI's Rule 59 surreply confirms there is no basis for a surreply regarding jury instructions, the exclusion of Mr. Pascarella's testimony, the exclusion of Fortress, or VLSI's statements regarding Mr. Stolarski's absence.

The impropriety of VLSI's Rule 59 surreply is further confirmed by VLSI's arguments responding to (1) jury instructions, (2) the exclusion of Mr. Pascarella's testimony, (3) the

[7] Although VLSI accuses Intel of "close-cropping" Dr. Sullivan's statement regarding allegedly "apportioned revenues" (Dkt. 629-2 at 6), the transcript speaks for itself. Dr. Sullivan compares numbers used in his damages calculation to the "***overall revenues***," calling them "a fraction -- think of it in a small piece, a sliver, if you will." (2/24 Tr. [Sullivan] 656:4-12.) This is exactly the type of statement prohibited by the Federal Circuit. (Dkt. 594 at 11; Dkt. 614 at 7.)

exclusion of Fortress evidence, and (4) VLSI's statements regarding Mr. Stolarski. In addressing each point, VLSI merely accuses Intel's reply brief of repeating "old arguments"—a fact which, even if true, would only confirm that VLSI had ample opportunity to address Intel's positions in VLSI's response brief. A surreply on these issues is not justified. (Dkt. 629-2 at 6-7.)

4. VLSI's Rule 59 surreply confirms there is no basis for a surreply to respond to Intel's explanation for why it is entitled to a new trial on infringement, invalidity, and damages.

Intel argued that multiple errors warranted a new trial on infringement, invalidity, and damages, and VLSI did not respond to those arguments in its opposition brief. (Dkt. 594 at 19-20; *see* Dkt. 614 at 10.) Now, after Intel noted VLSI's silence, VLSI responds—for the first time—in its surreply with a single conclusory statement. (Dkt. 629-2 at 7.) Not only is VLSI's response not a proper basis for a surreply, but it also does not rebut Intel's numerous explanations regarding why the errors here warrant a new trial on infringement, invalidity, and damages. (Dkt. 594 at 2, 4-7, 14-20.) For example, VLSI does not meaningfully respond to Intel's arguments that "damages are excessive and the verdict is the product of passion," that "the damages issues permeated the entire trial," or that the prejudicial errors affected Intel's entire case presentation. (*Id.* at 19-20.) As explained in Intel's new trial motion, the damages issues and evidentiary errors were intertwined with liability issues and undermined Intel's credibility, thus infecting the jury's judgment on liability issues as well as damages issues. (*Id.*)

IV. CONCLUSION

For the foregoing reasons, Intel requests that the Court deny VLSI's motion for leave.

Dated: June 4, 2021

Respectfully submitted,

/s/ *J. Stephen Ravel*

J. Stephen Ravel
Texas State Bar No. 16584975
Kelly Ransom
Texas State Bar No. 24109427
KELLY HART & HALLMAN LLP
303 Colorado, Suite 2000
Austin, Texas 78701
Tel: (512) 495-6429
Email: steve.ravel@kellyhart.com
Email: kelly.ransom@kellyhart.com

James E. Wren
Texas State Bar No. 22018200
1 Bear Place, Unit 97288
Waco, Texas 76798
Tel: (254) 710-7670
Email: james.wren@baylor.edu

Harry L. Gillam, Jr.
Texas State Bar No. 07921800
GILLAM & SMITH, L.L.P.
303 South Washington Avenue
Marshall, Texas 75670
Tel: (903) 934-8450
Email: gil@gillamsmithlaw.com

OF COUNSEL:
William F. Lee (*Pro Hac Vice)*
Louis W. Tompros (*Pro Hac Vice)*
Kate Saxton (*Pro Hac Vice*)
WILMER CUTLER PICKERING HALE & DORR LLP
60 State Street
Boston, Massachusetts 02109
Tel: (617) 526-6000
Email: william.lee@wilmerhale.com
Email: louis.tompros@wilmerhale.com
Email: kate.saxton@wilmerhale.com

Gregory H. Lantier (*Pro Hac Vice*)
Amanda L. Major (*Pro Hac Vice*)
WILMER CUTLER PICKERING HALE & DORR LLP
1875 Pennsylvania Avenue
Washington DC 20006
Tel: (202) 663-6000
Email: gregory.lantier@wilmerhale.com
Email: amanda.major@wilmerhale.com

Attorneys for Intel Corporation

CERTIFICATE OF SERVICE

I hereby certify that all counsel of record are being served with a copy of the foregoing document via electronic mail on June 4, 2021.

/s/ J. Stephen Ravel
J. Stephen Ravel